L14: Entry 6 of 19 File: USPT Mar 18, 2003

DOCUMENT-IDENTIFIER: US 6536034 B1
TITLE: Method for modifying code sequences and related device

Application Filing Date (1):
19990212

Brief Summary Text (17):
This object is achieved by the fact that the device for modifying code sequences comprises a second table TAB-SEC stored in the memory of the device and associating with each branch point (i) a time interval [.DELTA.Tmini; .DELTA.Tmaxi] associated with the time delay .DELTA.Ti prior to the execution of a new code sequence, and means for verifying that the time delay is authorized by the associated time interval supplied by this table.

CLAIMS:

4. The device for modifying code sequences according to claim 3, characterized in that it comprises a second table TAB_SEC stored in the memory of the device and associating with each branch point (i) a time interval [.DELTA.Tmini; .DELTA.Tmaxi] associated with the time delay .DELTA.Ti prior to the execution of a new code sequence, and means for verifying that the time delay is authorized by the associated time interval provided by this table.

16. The device for modifying code sequences according to claim 15, characterized in that it comprises a second table TAB_SEC stored in the memory of the device and associating with each branch point (i) a time interval [.DELTA.Tmini; .DELTA.Tmaxi] associated with the time delay .DELTA.Ti prior to the execution of a new code sequence, and means for verifying that the time delay is authorized by the associated time interval provided by said second this table.

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L14: Entry 15 of 19 File: USPT May 26, 1992

DOCUMENT-IDENTIFIER: US 5117387 A
TITLE: Microprogrammed timer processor

Application Filing Date (1):
19880818

Brief Summary Text (13):
The invention is carried out by a microprogrammed timer processor for servicing each of a plurality of input/output channels at a regularly recurring interval of time while concurrently performing other tasks comprising; storage circuitry means for storing a plurality of single instruction programs and a plurality of multiple instruction programs, clock circuitry defining sequential fetch and execute cycles within an instruction cycle, control circuitry responsive to said clock circuitry for interleaving single instruction programs with instructions in said multiple instruction programs so that a single instruction program may be executed while an instruction from a multiple instruction program is being fetched, said control circuitry including time interval setting circuitry which establishes an execution loop containing a predetermined number of said single instruction programs to be executed in sequence to fix said regularly recurring interval.

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L14: Entry 17 of 19 File: USPT Aug 22, 1978

DOCUMENT-IDENTIFIER: US 4109311 A
TITLE: Instruction execution modification mechanism for time slice controlled data processors

Application Filing Date (1):
19760923

CLAIMS:

1. In a data processing system, the combination comprising:

an instruction storage mechanism for storing instructions belonging to a plurality of different programs and including an address mechanism for accessing the stored instructions;

an instruction execution mechanism for receiving and executing the accessed instructions one at a time;

a time slice control mechanism for controlling the sequence in which the instructions are supplied to the execution mechanism for causing the instructions from the different programs to be executed in an interleaved manner by supplying them to the execution mechanism during interleaved time slice intervals and including circuitry for issuing a program identifier for each time slice interval and for supplying each program identifier to the instruction storage address mechanism for determining the program to be accessed during a particular time slice interval;

circuitry for supplying condition signals representing the occurrences of predetermined conditions in the data processing system;

and a function modification mechanism responsive to the occurrence of a predetermined program identifier and one of the condition signals for modifying the function of at least one of the instructions in the program identified by such program identifier.

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L16: Entry 1 of 2 File: USPT Nov 30, 1993

DOCUMENT-IDENTIFIER: US 5265944 A
TITLE: Wheel speed verification system

Application Filing Date (1):
19921228

Brief Summary Text (10):
In general, a combined brake and anti-skid controller for a wheeled vehicle has an anti-skid control circuit which includes an encoder for sensing rotation of a vehicle wheel and providing a first pulse train the repetition rate of which is indicative of the vehicle speed as well as a first processor for repetitively executing a sequence of program steps over a fixed time interval. The processor repeats the same predetermined sequence of program steps during each successive said fixed time interval. There is a second pulse train generator which is responsive to operation of the first processor for providing a second pulse train having one pulse for each repetition of the sequence of program steps. A second processor is instructed to compute wheel speed in response to a command from the first processor upon the first processor's detection of a certain wheel speed on a particular wheel. The second processor repetitively computes wheel speed specifically requested by the first processor. As an alternative, and in response to computation of a specific wheel speed by the first processor, a comparison of the specific wheel speed to the fixed time interval of the second processor may be effected and the anti-skid circuit allowed to continue in operation only so long as the compared specific wheel speed and time interval are within predetermined limits of one another.

Detailed Description Text (5):
In FIG. 2, the speed indicative signal on line 19 is also supplied to a counter 35 and then multiplied or divided by an appropriate scale factor (e.g. 8 as shown) so that the pulse rate supplied by scale factor circuit 39 to frequency comparator 41 is in wheel revolutions per second. Scale factors other than the number of pulses per revolution may, of course, be used in either the circuit of FIG. 1 or that of FIG. 2 depending on the particular instruction cycle rate of processor 17 and the wheel speed at which confirmation is desired. The instruction rate counter 37 also supplies a pulse train having a repetition rate of one pulse per complete execution of the instruction set of the failsafe microprocessor 17. If the comparator 41 indicates the two pulse trains have the same (within limits) repetition rates, the antilock feature is allowed to continue, but if the comparison is not within safe limits, a signal on line 43 disables the antilock feature as before.

Detailed Description Text (7):
There are numerous particular ways in which the process of confirming wheel speed determination at a particular wheel speed may be accomplished. For example, the main microprocessor 15 detects the wheel speed (perhaps in MPH, RPM, or as a pulse train of specified repetition rate) that correlates with the known failsafe microprocessor 17 software execution loop time whereupon, the processor 15 sends a "verify wheel speed" command to processor 17. Processor 17 looks for a single transition during each software loop at the scale factor 39 output. These translations may be counted by the processor 17 and the number of transitions over

a period of time should be the same as the number of software loops. If those two numbers differ by more than some prescribed limits, anti-skid operation is interrupted.

CLAIMS:

5. In an anti-skid control circuit for a wheeled vehicle, a method of processor computation confirmation where confirmation occurs only at a certain one of computation values, comprising the steps of:

sensing rotation of at least one vehicle wheel and providing a pulse train a repetition rate of which is indicative of vehicle speed;

repetitively executing a predetermined sequence of program steps in a microprocessor over a fixed time interval, the microprocessor repeating the predetermined sequence of program steps during successive fixed time intervals;

repetitively computing the speed of said at least one vehicle wheel in response to the pulse train;

comparing the computed wheel speed to said fixed time interval and allowing the anti-skid control circuit to continue in operation only so long as the compared wheel speed and time interval are within predetermined limits of one another, the comparison being effected only at a certain specific wheel speed.

6. In an anti-skid control circuit for a wheeled vehicle, a method of processor computation confirmation where confirmation occurs only at a certain one of computation values, comprising the steps of:

sensing rotation of at least one vehicle wheel and providing a first pulse train a repetition rate of which is indicative of vehicle speed;

repetitively executing a predetermined sequence of program steps in a microprocessor over a fixed time interval, the microprocessor repeating the predetermined sequence of program steps during successive fixed time intervals;

providing a second pulse train having one pulse for each repetition of the sequence of program steps;

repetitively computing the speed of said at least one vehicle wheel according to the repetition rate of the first pulse train; and

comparing the repetition rates of the first and second pulse trains and initiating corrective action in the event that the compared repetition rates differ by more than a prescribed amount, the comparison being effected only at a certain specific wheel speed.

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